REMARKS

This is a response to the Office Action mailed July 27, 2005. The Office Action objected to claim 20, rejected claims 28-30 under 35 U.S.C. §112, rejected claims 15, 17-19, 20, 24, 28, 29, 31, and 32 under 35 U.S.C. §102, and rejected claims 23 and 30 under 35 U.S.C. §103(a), and noted the allowability of claims 1-6, 8, 9, 11, 16, 21, 22, and 27.

Claims 1, 5, 15, 20, 35, 37, and 39 have been amended. Claims 4, 21, 28, 29, 33, 34, 36, and 38 have been cancelled. Claims 41 and 42 have been added. Claims 1-3, 5-6, 8-9, 11-12, 15, 20, 23, 24, 30, 35, 37, and 39-42 remain pending in this application.

Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Premature Finality of the Office Action

Applicants respectfully submit that the finality of the Office Action was premature.

Under MPEP § 706.07(a), "A second or any subsequent action on the merits in any application ... should not be made final if it includes a rejection, on prior art not of record, of any claim amended to include limitations which should reasonably have been expected to be claimed."

In the Office Action of April 20, 2005, the Examiner indicated that claims 1-6, 8, 9, 11, and 12 where allowed and claims 16, 21, 22, and 27 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims. Independent claims 15 and 20 were amended to include the novel limitations of claims 16 and 21. It is respectfully submitted that in view of the indication of allowance and allowable subject matter in these claims and the directions for amendment, the Examiner should have reasonably

expected that such amendments would be carried out, and that the Final Rejection is therefore premature under MPEP § 706.07(a).

Also under MPEP § 706.07(a), a second or subsequent action on the merits "shall be final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement...." As to independent claims 1 and 5, which were previously allowed, the Examiner relies on a new ground of rejection (i.e., Hayasaka et al. – U.S. Pat. No. 6,809,421) which was not previously cited by the Examiner and was not submitted in an information disclosure statement by the Applicants. As to independent claims 15, 20, and 35 which were amended or added to include the previously allowable subject matter of claims 16 and 21, the Examiner also relies on Hayasaka et al. as a new ground for rejection. It is respectfully submitted that the new ground of rejection (i.e., Hayasaka et al.) was not necessitated by Applicants' amendment, and it is therefore the finality of the rejection of independent claims 1, 5, 15, 20, and 35, and their dependent claims, was premature and should be withdrawn.

Objections

The Office Action objected to claims 33 and 40 as informal due to a minor grammatical error. Applicants have amended claims 33 and 40 to correctly the informalities noted in the Office Action. Withdrawal of this objection is respectfully requested.

Rejections Under 35 U.S.C. § 112

The Office Action rejected claims 29 and 35-38 under 35 U.S.C. §112, ¶2, as being indefinite. Applicants have amended claims 29 and 35-38 to correct the problems noted in the Office Action. Applicants respectfully request that this rejection be withdrawn.

Rejections Under 35 U.S.C. § 102

The Office Action rejected claims 15, 20, 28, and 35 under 35 U.S.C. §102(e) as being anticipated by Hayasaka et al. (U.S. Pat. No. 6,809,421) ("Hayasaka").

As to independent claims 15, 20, and 35, Applicants have amended these claims to literally or substantively include the limitations - "identical chip-scale packages arranged in a stacked configuration", "five sides of the semiconductor device are completely exposed and a sixth side of the semiconductor device is partially exposed for improved heat dissipation", and "substrate made from a different material than the semiconductor device." Applicants submit that none of these limitations are found in Hayasaka or any of the cited prior art references.

As seen in Fig. 33 of Hayasaka, the chip stack includes two chips in one layer 152_2 and one chip in another layer 152_1. Thus, these are not identical chip-scale packages as claimed. Additionally, Hayasaka teaches the use of an adhesive 169 between one surface of the chip 151 and the substrate 152. (See Col. 26, lines 5-14) The present invention, on the other hand, uses no adhesive or filler on any surface of the semiconductor device to improve heat dissipation and maintains all six surfaces of the semiconductor device fully or partially exposed. Thus, Hayasaka fails to meet this limitation. Additionally, Hayasaka teaches that the semiconductor device and substrate are both made of silicon to match their coefficient of thermal expansion. (See Col. 26, lines 8-14). The present invention on the other hand claims that the semiconductor device and substrate are made of different materials yet have coefficient of expansions of within six parts per million per degree Celsius or less of each other. It is important to note that because of its properties, silicon substrates are disfavored in some implementations. The present invention addresses such issue by providing relatively close coefficients of expansion while using different materials. Thus, Hayasaka also fails to teach this limitation.

As a result of these amendments, Applicants submit that independent claims 15, 20, and 35, and their dependent claims are in condition of allowance.

The Office Action also rejected claims 35-38 under 35 U.S.C. §102(b) as being anticipated by Bertin et al. (U.S. Pat. No. 5,977,640) ("Bertin").

Independent claims 35 and 37 have been amended to literally or substantively include the limitations - "the first surface [of the memory device] is partially exposed and the other five surfaces of the memory device are completely exposed for improved heat dissipation" and "the substrate [is] made from a different material than the memory device." Applicants submit that neither of these limitations are found in Bertin or any of the cited prior art references.

The Office Action relies on chip 30 in Bertin as being the claimed "substrate." However, the common meaning of a substrate is that of a surface on which circuits can be laid-out and components attached thereto. The chip 30 is simply not a "substrate" as claimed since it has a different function than a simple substrate. Usually, chips are designed to process information, not act as a surface for coupling other components. Even if another chip 40 can be coupled to interface points of the chip 30, it does not make this chip 30 a substrate. Additionally, as amended, the claimed substrate and memory device are made of different materials. In Bertin, the material of chips 40 and 30 is the same. Moreover, Bertin appears to teach that the chips are encapsulated (Fig. 5, item 64; Col. 3, lines 62-65). The present claim, on the other hand, recites that the memory device is completely exposed on five sides and partially exposed on the sixth side. Thus, Bertin fails to teach the invention as claimed.

The Office Action rejected claims 39 and 40 under 35 U.S.C. §102(e) as being anticipated by Kasatani (U.S. Pat. No. 6,617,695) ("Kasatani").

Independent claim 39, as amended, recites "memory die ... having a first surface, the first surface of the memory die mounted facing the first surface of the substrate, wherein the first surface of the memory die remains partially exposed and the other five surfaces of the semiconductor device are completely exposed." The Office Action relies on item 17 in Kasatani as teaching the memory die with exposed surfaces as claimed. However, a close reading of Kasatani shows that item 17 is actually an integrated circuit package including package body 18. (See Col. 7, lines 10-14). Unlike the present claimed invention which claims a "memory die" (which is a circuit without packaging), Kasatani teaches a packaged circuit 17. Because of its packaging 18, the circuit is not fully exposed on five surfaces as claimed. In fact, the packaged circuit 17 is completely encapsulated, which is what the present claimed invention avoids. Thus, Kasatani fails to teach the invention as claimed.

Rejections Under 35 U.S.C. § 103

The Office Action rejected claims 1-3, 5, 6, 8, 9, 11, 12, 23, and 30 under 35 U.S.C. §103(a) as being unpatentable over Hayasaka et al. (U.S. Pat. No. 6,809,421) ("Hayasaka") in view of Nishimura et al (U.S. Pat. No. 6,781,241) ("Nishimura").

As to independent claims 1 and 5, Applicants have amended these claims to literally or substantively include the limitations "five sides of the memory die are completely exposed and a sixth side of the memory die is exposed for improved heat dissipation" and "the substrate made from a different material than the memory die." Hayasaka teaches the use of an adhesive 169 between one surface of the chip 151 and the substrate 152. (See Col. 26, lines 5-14) The present invention, on the other hand, uses no adhesive or filler on any surface of the semiconductor device to improve heat dissipation and maintains all six surfaces of the semiconductor device

fully or partially exposed. Thus, Hayasaka fails to meet this limitation. Additionally, Hayasaka teaches that the semiconductor device and substrate are both made of silicon to match their coefficient of thermal expansion. (See Col. 26, lines 8-14). The present invention claims that the semiconductor device and substrate are made of different materials yet have coefficient of expansions of within six parts per million per degree Celsius or less of each other. Thus, Hayasaka also fails to teach this limitation.

The Office Action also rejected claims 4, 33, and 34 under 35 U.S.C. §103 (a) as being unpatentable over Hayasaka in view of Nishimura and further in view of Kelly et al. (U.S. Pat. No. 5,798,567) ("Kelly").

Regarding Kelly, Applicants note that it fails to teach "five sides of the memory die are completely exposed and a sixth side of the memory die is exposed" since an adhesive 59 is used to fully cover one surface of the memory die 41. (See Fig. 4). Thus, Hayasaka in view of Kelly fail to teach the invention as claimed.

The Office Action also rejected claims 21, 29, and 36 under 35 U.S.C. §103 (a) as being unpatentable over Hayasaka in view of Kelly et al. (U.S. Pat. No. 5,798,567) ("Kelly").

While Applicants disagree that the cited references teach the claimed invention, this argument need not be reached since claims 21, 29, and 36 have been cancelled.

The Office Action also rejected claim 24 under 35 U.S.C. §103 (a) as being unpatentable over Hayasaka in view of Corisis et al. (U.S. Pat. No. 6,414,391) ("Corisis").

While Applicants disagree that the cited references teach the claimed invention, this argument need not be reached since claim 24 has been cancelled.

Applicants submit that as a result of the amendments made to the independent claims and the remarks distinguishing the prior art, the remaining claims are in condition for allowance.

Applicants submit herewith an Information Disclosure Statement which require payment of the fee as set forth in 37 CFR 1.17(p). Please charge any other necessary fee for consideration of the Information Disclosure Statement to Deposit Account No. 19-2090.

It is believed that this Disclosure complies with the requirements of 37 CFR 1.56 and the MPEP. If the some reason the Examiner thinks otherwise, he is asked to call the undersigned so that any deficiencies can be remedied.

CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited. Authorization is hereby given to charge our Deposit Account No. 19-2090 for any charges that may be due. Furthermore, if an extension is required, then Applicants hereby request such an extension.

Respectfully submitted,

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I hereby certify that this document is being deposited on September 27, 2005 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313

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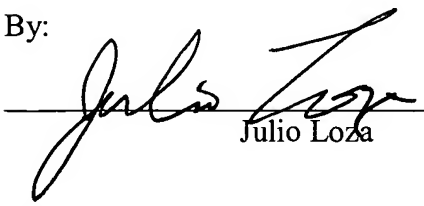

Julio Loza

Dated: September 27, 2005